

# EUROPEAN PATENT OFFICE

## Patent Abstracts of Japan

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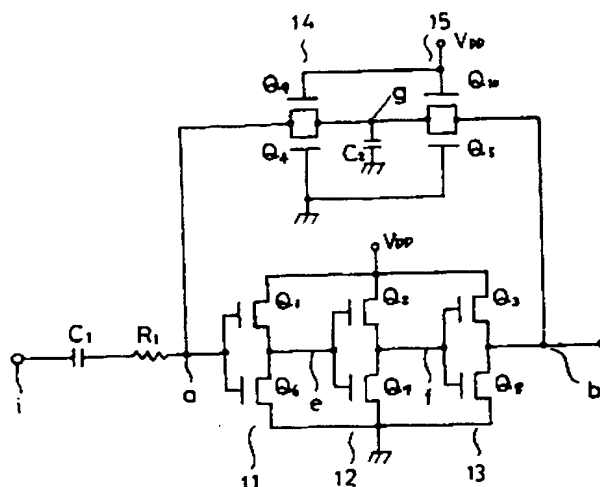
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INVENTOR : MURAWAKI KENICHI;

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TITLE : COMPLEMENTARY MOS TRANSISTOR  
CIRCUIT



ABSTRACT : PURPOSE: To obtain an oscillation amplifier oscillated and amplified normally to a minute amplitude signal while suppressing a through-current by connecting plural stages of inverters in series and connecting a large capacitance load to the intermediate point of a feedback resistor to the inverter connection.

CONSTITUTION: Transistors (TR)  $Q_4$ ,  $Q_9$ ,  $Q_5$  and  $Q_{10}$  of transfer gate type acting like feedback resistors are arranged in series between an input point (a) of the 1st stage inverter 11 and an output point (b) of the 3rd stage inverter 13. The feedback resistor is divided into two, a large capacitance load  $C_2$  is connected to the midpoint (g) to form a delay circuit. Thus, a proper delay time is applied to a large amplitude waveform at the point (b) to a degree giving an effect onto the input section of the point (a). Thus, the effect of the output section onto the input is prevented by providing a delay means having a large time constant to an input signal frequency to a feed back section.

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